As the three-month shortened statutory period for reply is due March 21, 2005, this Response is therefore considered timely filed.

AMENDMENTS

In the Specification

Please amend the specification as indicated in the replacement paragraphs below. Applicants respectfully submit that no new matter has been added to the specification. Applicants respectfully request that the amendments shown in the replacement paragraphs be accepted and entered into the file of the above styled case.

In the Claims

Please cancel claims 1-26 without prejudice to file same in a continuation, continuation-in-part, divisional or co-pending application, and amend the remaining claims as indicated below.

Applicants respectfully submit that no amendments have been made to the pending claims for the purpose of overcoming any prior art rejections that would restrict the literal scope of the claims or equivalents thereof.

REPLACEMENT PARAGRAPHS FOR THE SPECIFICATION SHOWING AMENDMENTS MADE THERETO

Please replace the paragraphs at page 8, lines 3-6 with the following replacement paragraphs (indicating amendments thereto):

~~Figure 3 illustrates a~~ Figures 3a-3d illustrate schematic ~~diagram~~ diagrams of various exemplary bistable memory devices, according to the exemplary embodiment of Figure 2;

~~Figure 4 illustrates~~ Figures 4a and 4b illustrate schematic block diagrams of exemplary digital processors, according to the exemplary embodiment of Figure 2;

Please replace the paragraphs starting at page 9, line 20 to page 11, line 15 with the following replacement paragraphs (indicating amendments thereto):

Referring to Figure 2, depicted is a schematic block diagram of an event detector, according to an exemplary embodiment of the invention. The event detector is generally depicted by the numeral 200 and comprises a bistable memory device 204 and a digital processor 206. ~~Figure 3 illustrates~~ Figures 3a-3d illustrate various exemplary bistable memory devices 204. The bistable memory device 204a is an R-S flip-flop (Figure 3a), device 204b is a D flip-flop (Figure 3b), device 204c is a J-K flip-flop (Figure 3c), and device 204d is a counter (Figure 3d). It is contemplated and within the scope of the present invention that the bistable memory device 204 may be any device that will toggle and retain its output state when an event 102 is detected on its input, e.g., toggle flip-flop, latch, counter (synchronous and asynchronous) and the like. The output 208 of the bistable memory device 204 is at a logic state of either a first logic level or a second logic level. Each time an event 102 is detected the logic state at the output 208 changes. Thus the logic state of the output 208 alternates between the first and second logic levels for each event 102.

Referring to ~~Figure 4~~ **Figures 4a and 4b**, depicted are block diagrams of exemplary digital processors. **As depicted in Figure 4a, the** **[[The]]** digital processor 206a may comprise a central processing unit (CPU) 422, a read only memory (ROM) 424, a random access memory (RAM) 426 and input-output (I/O) 428. The CPU 422 reads the logic state of the output 208 and compares the logic level of the logic state read to a stored logic level of a previously read logic state. If the logic level of the logic state read and the logic level stored from the previously read logic state are the same, then no event has occurred during the time between the read and previous read of the logic states of the bistable memory device. If different, then an event has occurred during the time between the read and previous read logic states of the bistable memory device.

In another embodiment depicted in Figure **[[4]]** **4b**, the digital processor 206b may comprise digital logic gates and a storage register such as, for example but not limited to, a flip-flop 452. The bistable memory device 204 (Figure 2) is represented by a D flip-flop 204b (Figure **[[3]]** **3b**) having a Q output 208 connected to an input of the flip-flop 452. The logic state at the Q output 208 of the flip-flop 204b consists of two logic levels, a first logic level and a second logic level. The first logic level may be a logic high and the second logic level may be a logic low, or visa-versa. For example, an event 102 toggles the logic state of the output 208 to the first logic level. A next event 102' toggles the logic state of the output 208 to the second logic level. A subsequent event 102" toggles the logic state of the output 208 back to the first logic level, etc. The logic state of the output 208 remains at one of the two logic levels irrespective of whether the event 102 is momentary or of short duration. The event 102 may also be depicted as a transition from a logic low to a logic high, or a logic high to a logic low

(referred to herein as "edge triggering"). Thus a constant logic level of the logic state at the output 208 of the flip-flop 204b is maintained between detection of events.